REMARKS

This application has been carefully reviewed in light of the Office Action dated June 2, 2006. Claims 1 to 15 remain pending in the application, of which Claims 1, 6 and 11 are independent. Reconsideration and further examination are respectfully requested.

Claims 1 to 15 were rejected under 35 U.S.C. § 102(b) over U.S. Patent No. 5,661,373 (Nishizawa). Reconsideration and withdrawal of the rejections are respectfully requested.

The present invention controls the release of a data signal line of a serial communication apparatus in which one data signal line is used for both sending and receiving signal data. According to the invention, a controller controls a buffer to release the data signal line after the data signal line is temporarily retained at a second level, if a control signal for instructing a release of the data signal line for receiving data through the data signal line is input when data is sent through the one data signal line at a first level. In other words, when a mode to send a data signal is switched to a mode to receive a data signal, a control signal for instructing the release of the data signal line is input. By virtue of the foregoing, since the data signal line for receiving data is released after the data signal line has been temporarily retained at the second level, a blunt waveform of a signal can be prevented.

Referring specifically to the claims, amended independent Claim 1 is directed to a serial communication apparatus in which one data signal line is used for both sending and receiving signal data, comprising buffer means for releasing the data signal line for receiving data through the data signal line, and control means for controlling the

buffer means to release the data signal line after the data signal line is temporarily retained at a second level if a control signal for instructing a release of the data signal line for receiving data through the data signal line is input when data is sent through the one data signal line a first level.

Claim 6 is a method claim that substantially corresponds to Claim 1, while Claim 11 is an apparatus claim corresponding to Claim 1, but is written in non-means-plus-function format.

The applied art is not seen to disclose or to suggest the features of independent Claims 1, 6 and 11, and in particular, is not seen to disclose or to suggest at least the feature of controlling a buffer to release a data signal line, which is used for both sending and receiving signal data, after the data signal line is temporarily retained at a second level, if a control signal for instructing a release of the data signal line is input when data is sent through the one data signal line at a first level.

Nishizawa merely discloses a method for transmitting binary digital signals in which a signal line is used for one way communication. This is readily evident from Fig. 2 of Nishizawa, and particularly, arrows A1 and A2 which show a current flow direction in each signal line. This implies that the terminal TRT only sends a binary digital signal via one signal line, and uses a separated signal line to receive signals. Thus, Nishizawa is not seen to disclose a serial communication apparatus in which one data signal line is for both sending and receiving a signal data.

Additionally, Nishizawa discloses that binary digital signals are transmitted by using two kinds of pulses; one of which has a sharp waveform at the leading edge and a blunt sharp waveform at the trailing edge of the pulse, and the other of which has a blunt

waveform at the leading edge and a sharp waveform at the trailing edge of the pulse. A three-state buffer is used for generating those kinds of pulses. Thus, Nishizawa merely teaches the use of a three-state buffer. However, Nishizawa is not seen to disclose or to suggest controlling a buffer to release a data signal line, which is used for both sending and receiving signal data, after the data signal line is temporarily retained at a second level, if a control signal for instructing a release of the data signal line is input when data is sent through the one data signal line at a first level.

In view of the foregoing deficiencies of Nishizawa, Claims 1 to 15 are not believed to be anticipated. Accordingly, Claims 1 to 15 are believed to be allowable.

No other matters having been raised, the entire application is believed to be in condition for allowance and such action is respectfully requested at the Examiner's earliest convenience.

Applicants' undersigned attorney may be reached in our Costa Mesa, California office at (714) 540-8700. All correspondence should continue to be directed to our below-listed address.

Respectfully submitted,

/Edward Kmett/

Edward A. Kmett
Attorney for Applicants
Registration No.: 42,746

FITZPATRICK, CELLA, HARPER & SCINTO
30 Rockefeller Plaza
New York, New York 10112-3800
Facsimile: (212) 218-2200

CA_MAIN 122810v1